Router Chip

ECE 122 Final Presentation

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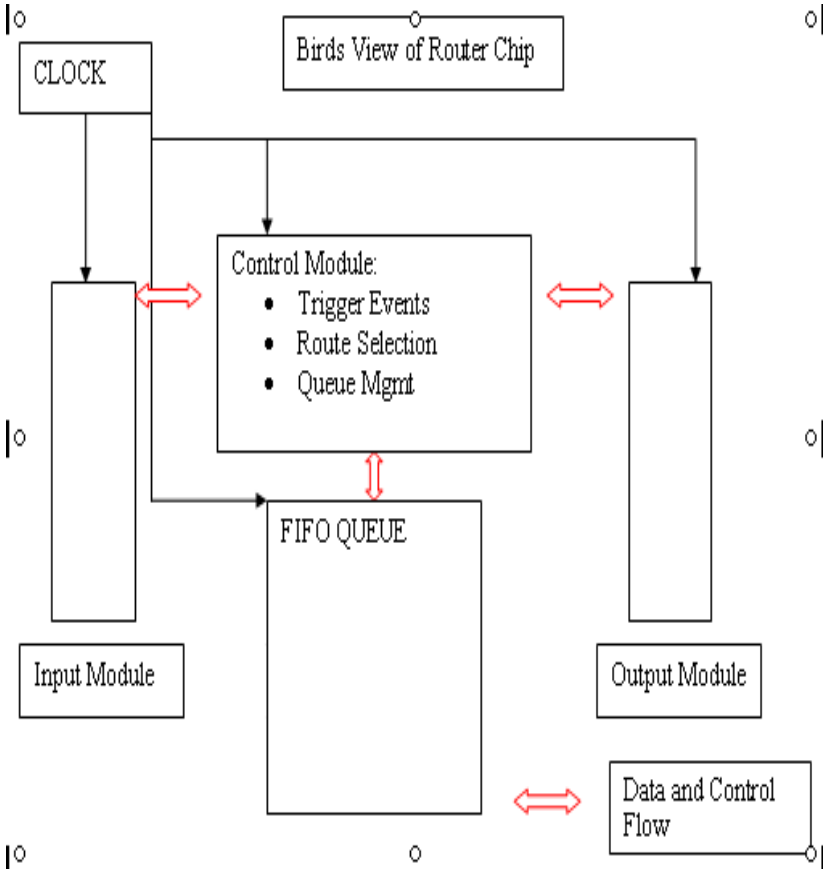
Functions of the Router

- Accept serial data in and serial data out
- Frame delimiting and Header processing
- Queuing of low priority packets or on BUSY destination.
- Processing time for routing should be minimized
- Operate on Maximum possible clock speed to increase the data throughput

Router Chip - Modules

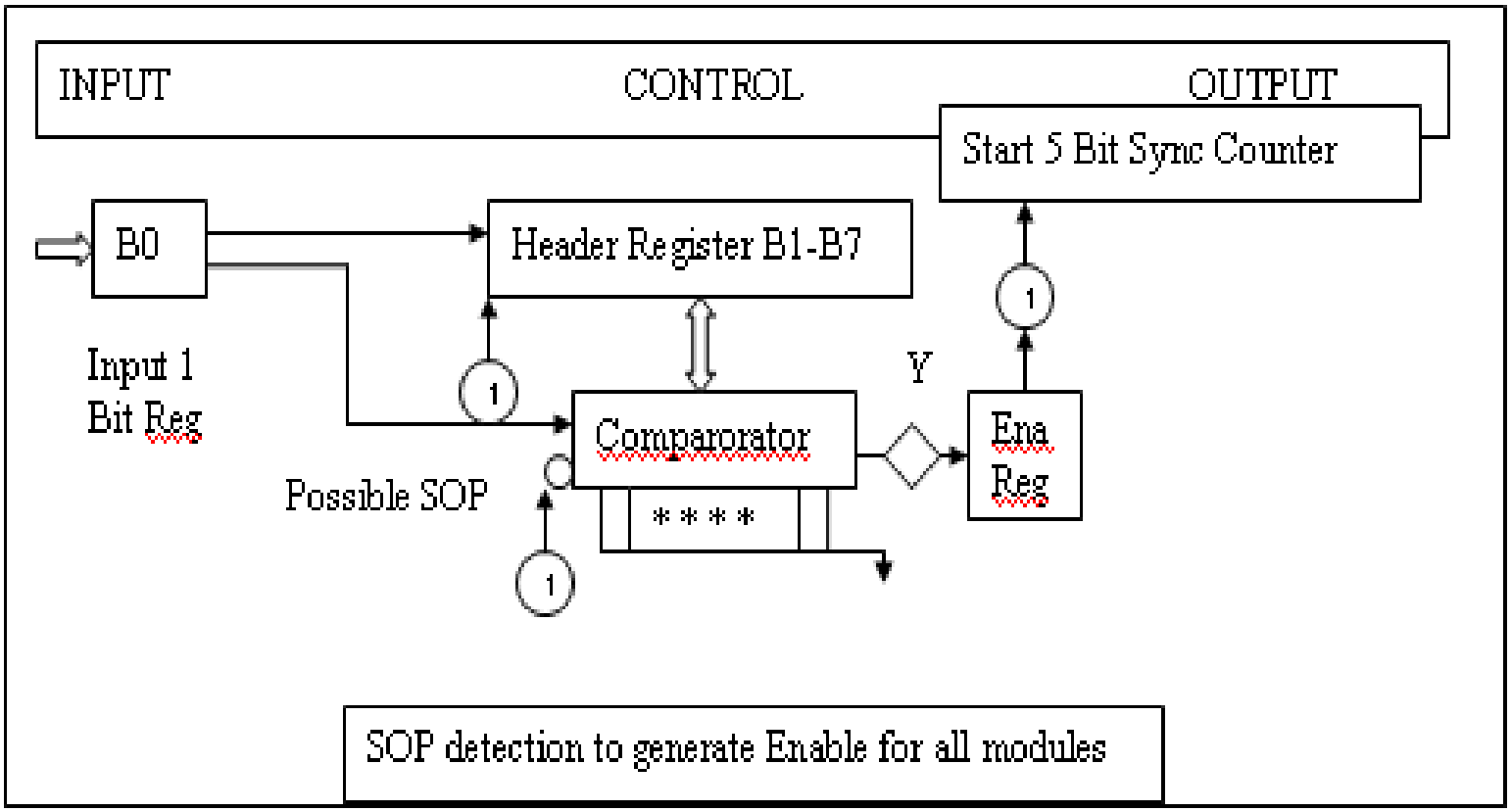
- The Clock Module provides the reference timing
- The Input and Output modules interfaces to the external world
- The Controller Module is the brain of the system



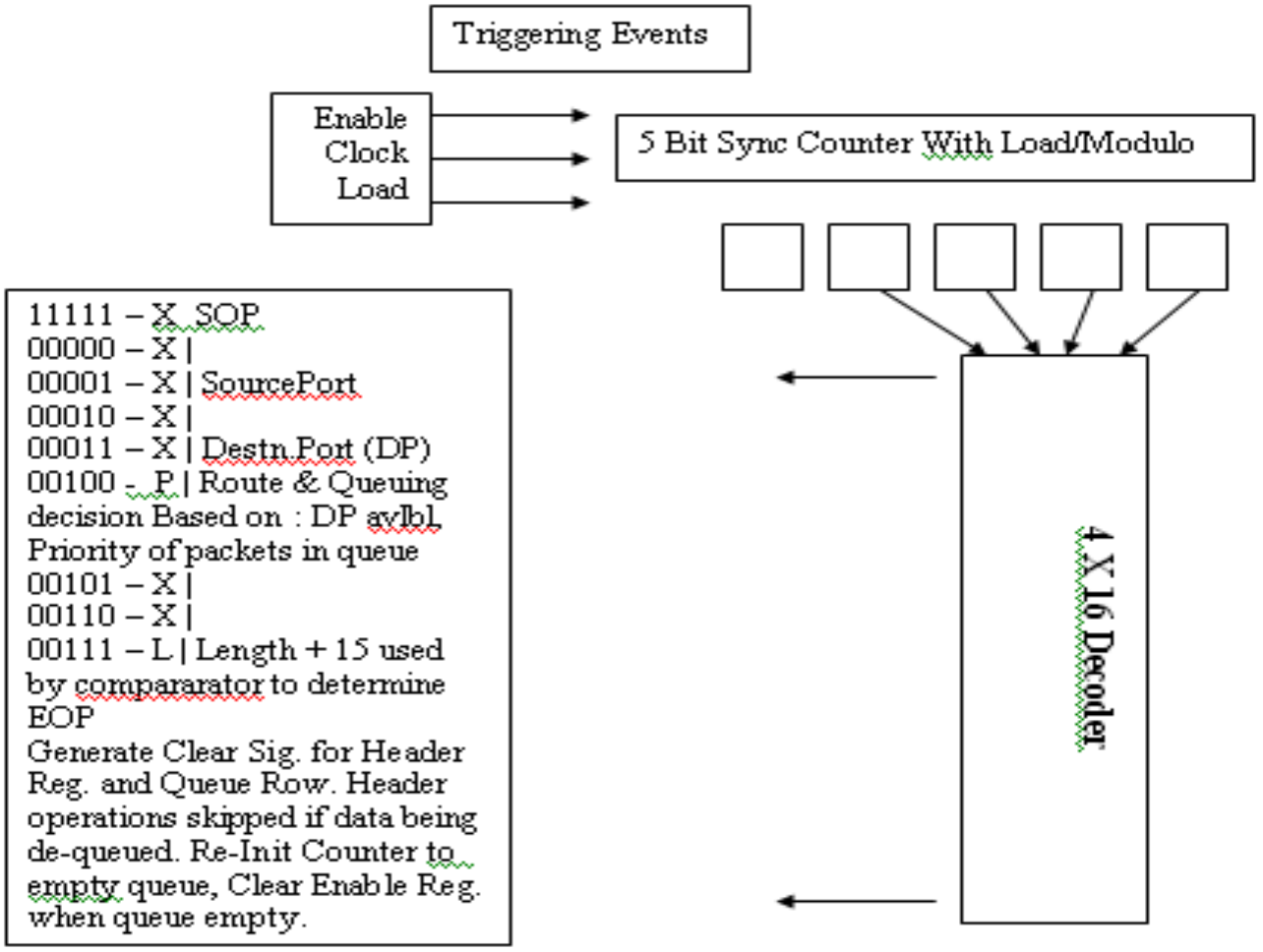
State and Event based response

- The Controller Triggers and Handles Events
- Does the Lookup for Routing and Queuing
- Generates signals (Enable) or controls data flow
- The controller uses a counter to trigger events.
- It uses a comparorator (bit-wise xor) for looking up particular values.
- Decoders are used to trigger events based on the counted clock pulses.
- Multiplexers are used to control the data flow.

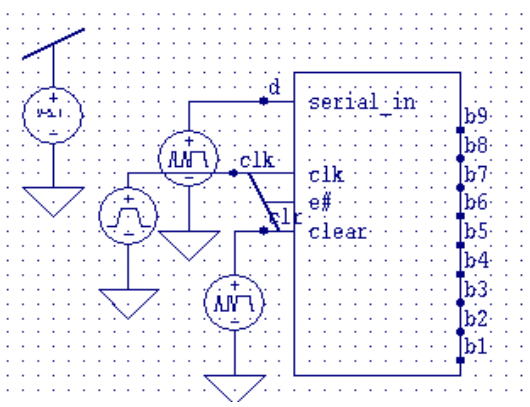
SOP Triggered Event

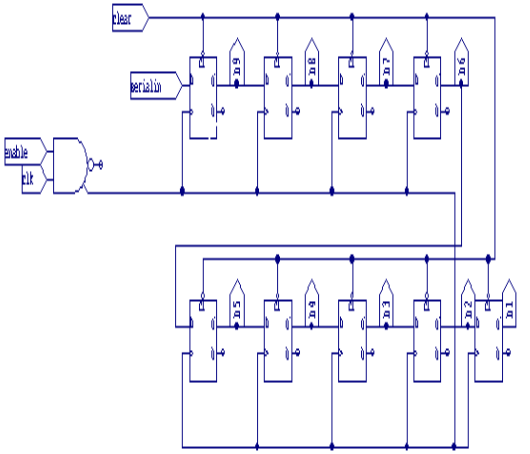


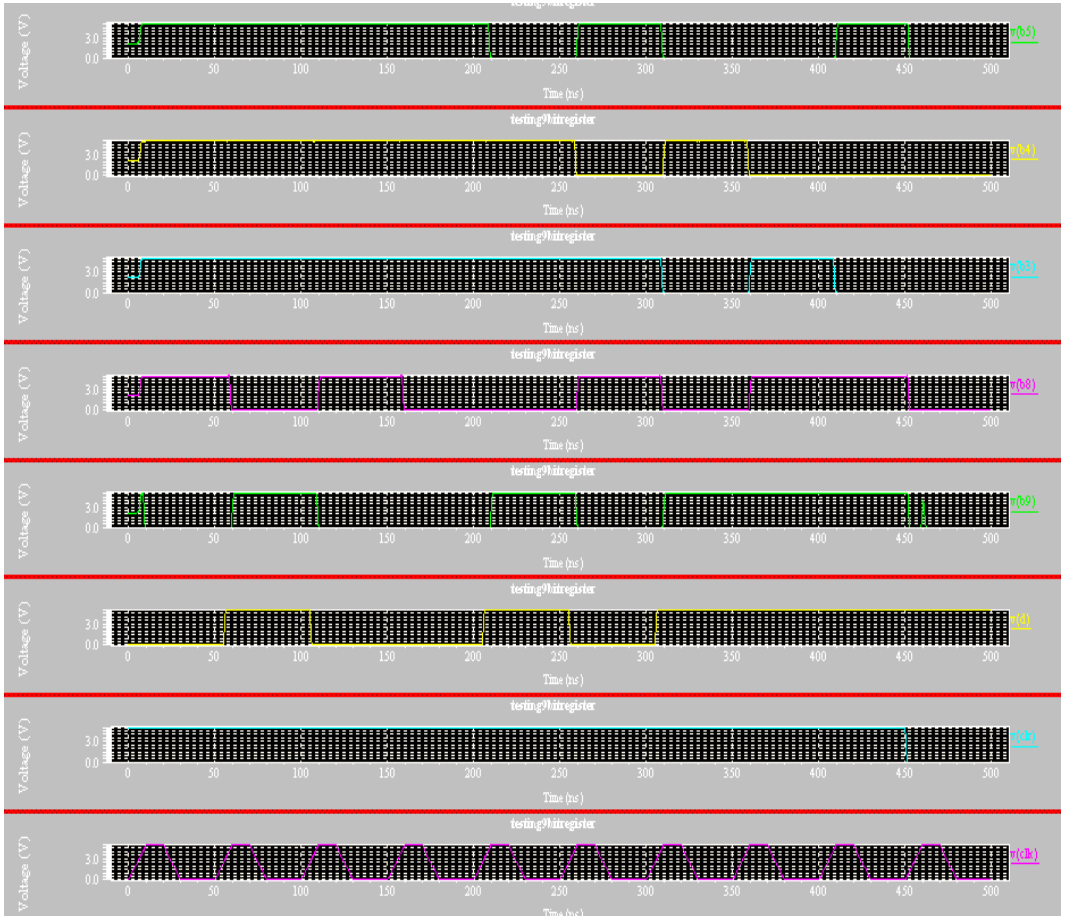
Clocked Events



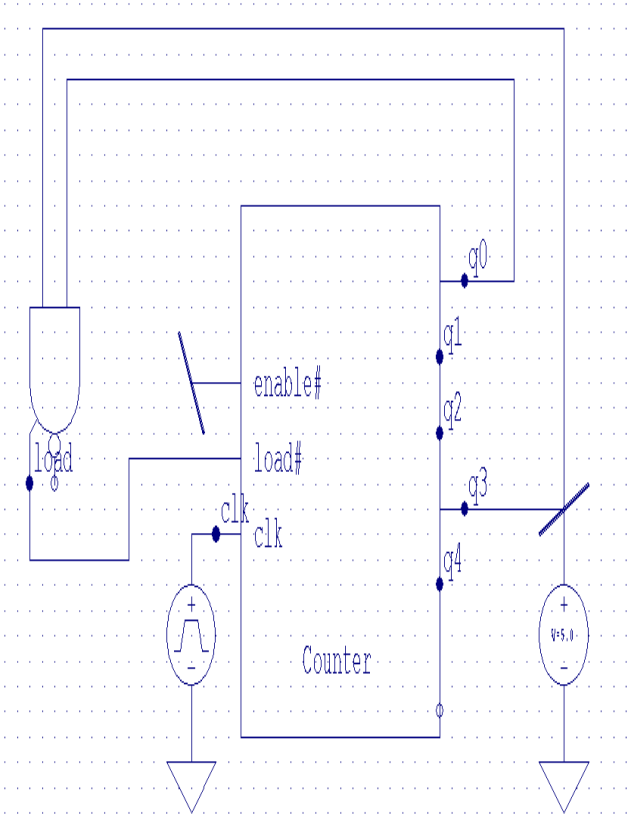
Header Register With Clear

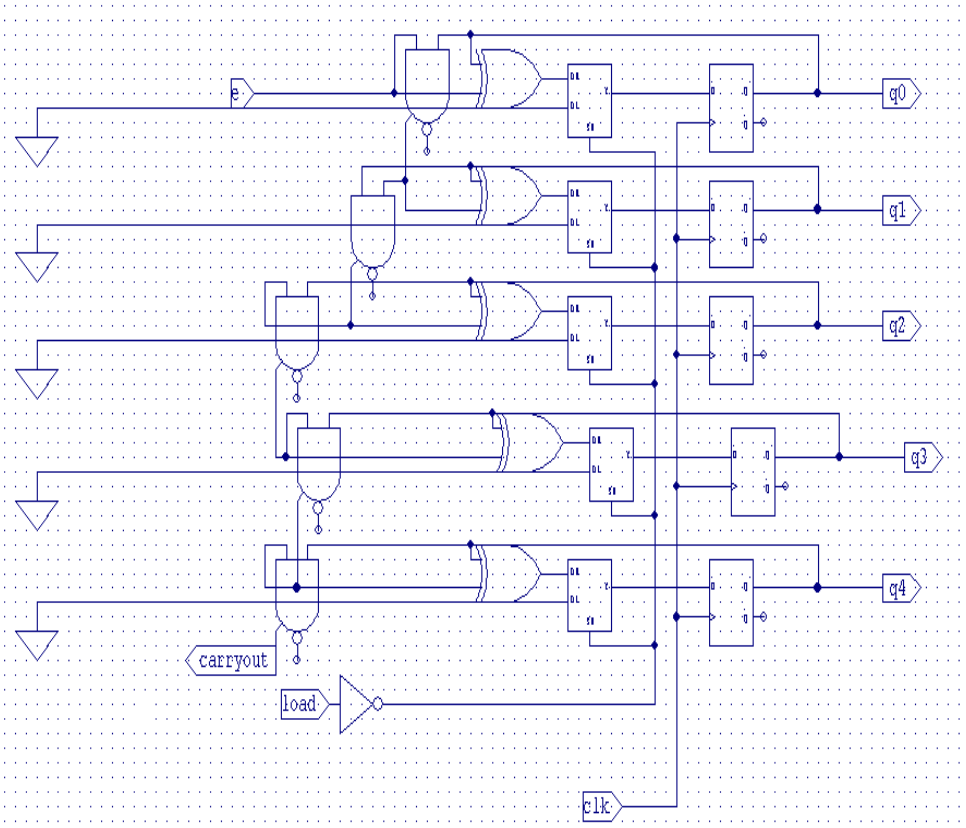




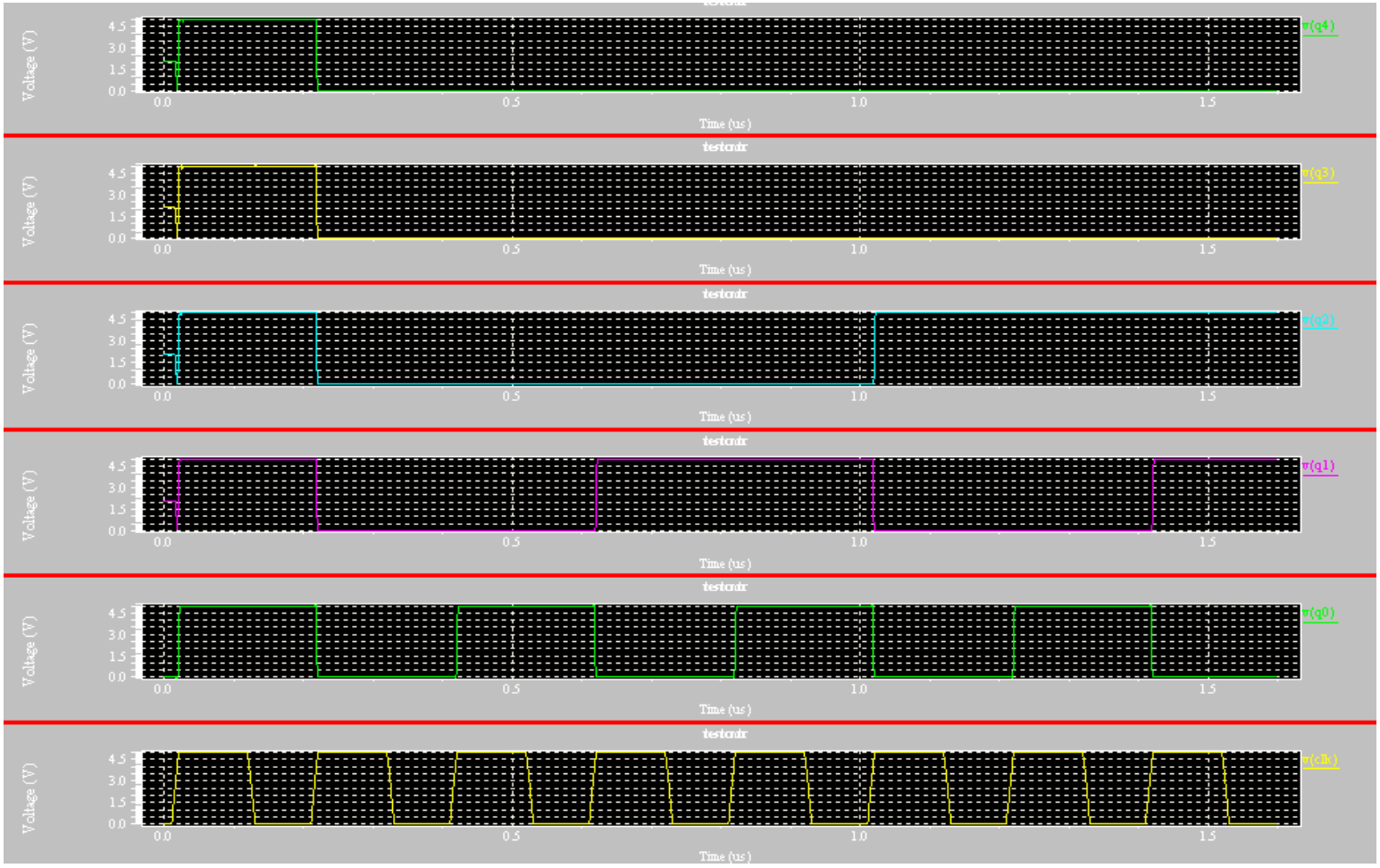


Five Bit Synchronous Counter with modulo operation

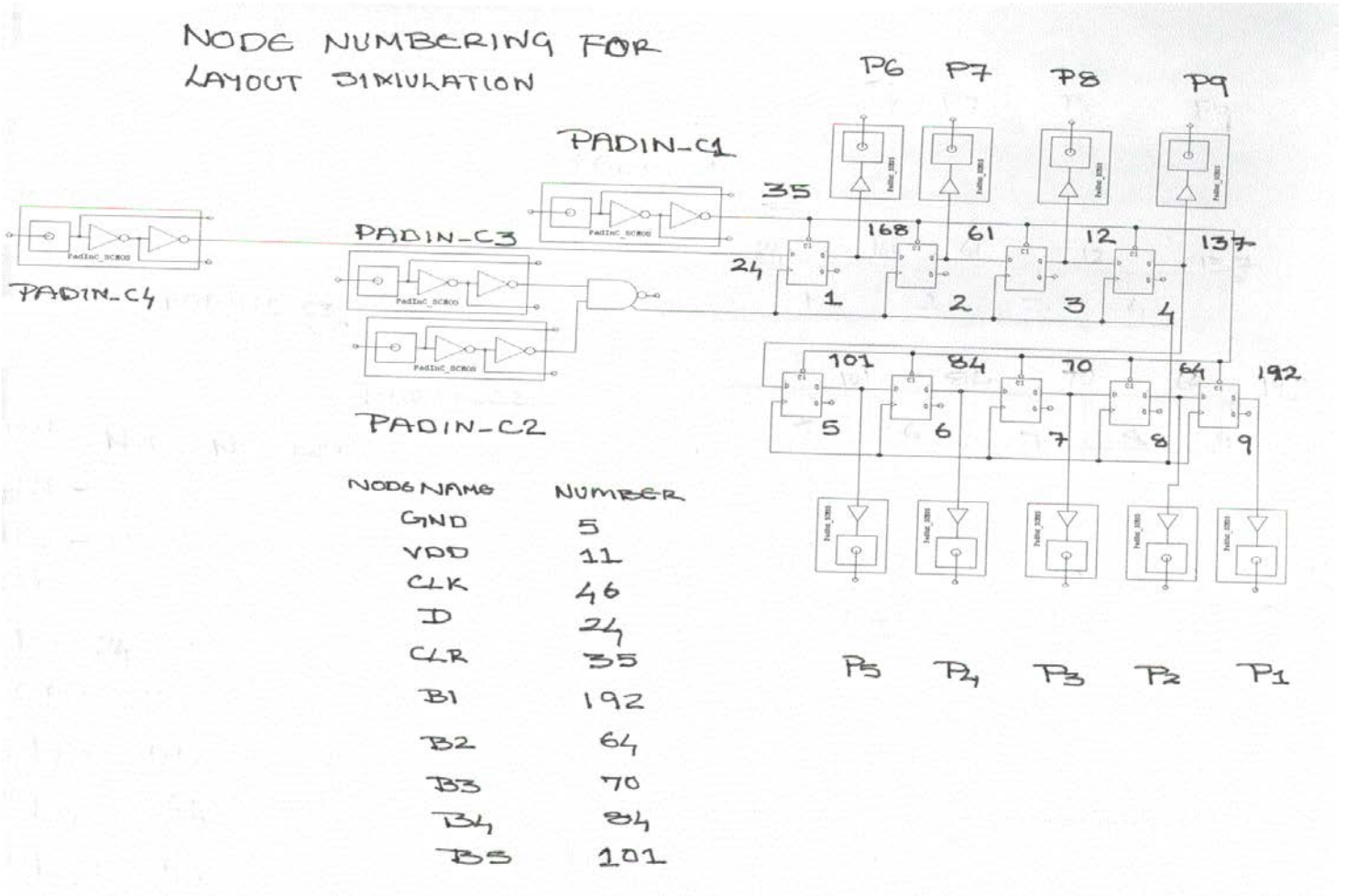




Counter Operation



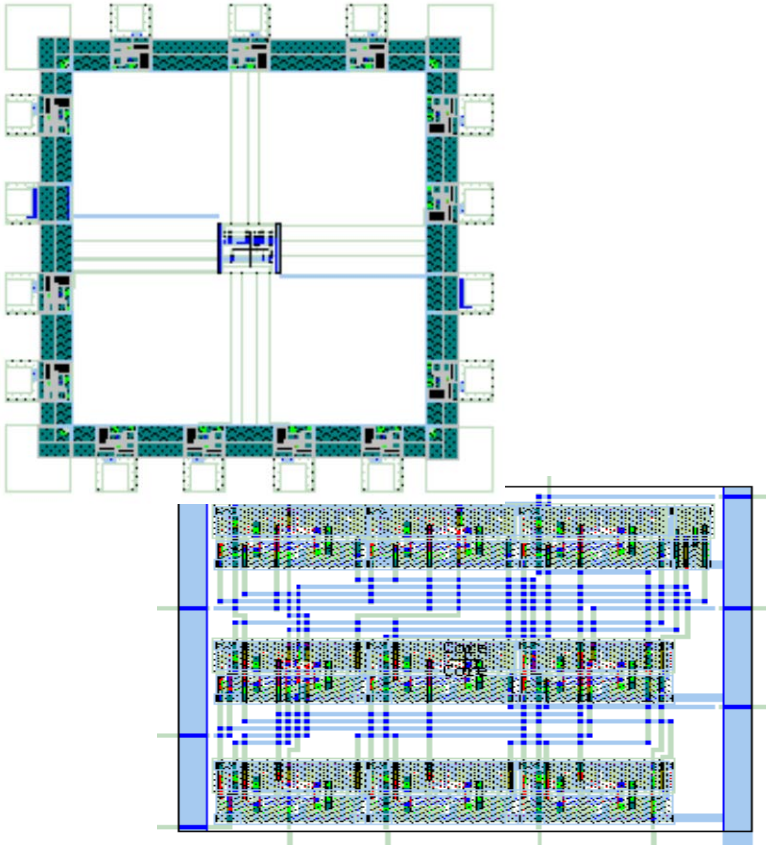
Node Identification From Extract



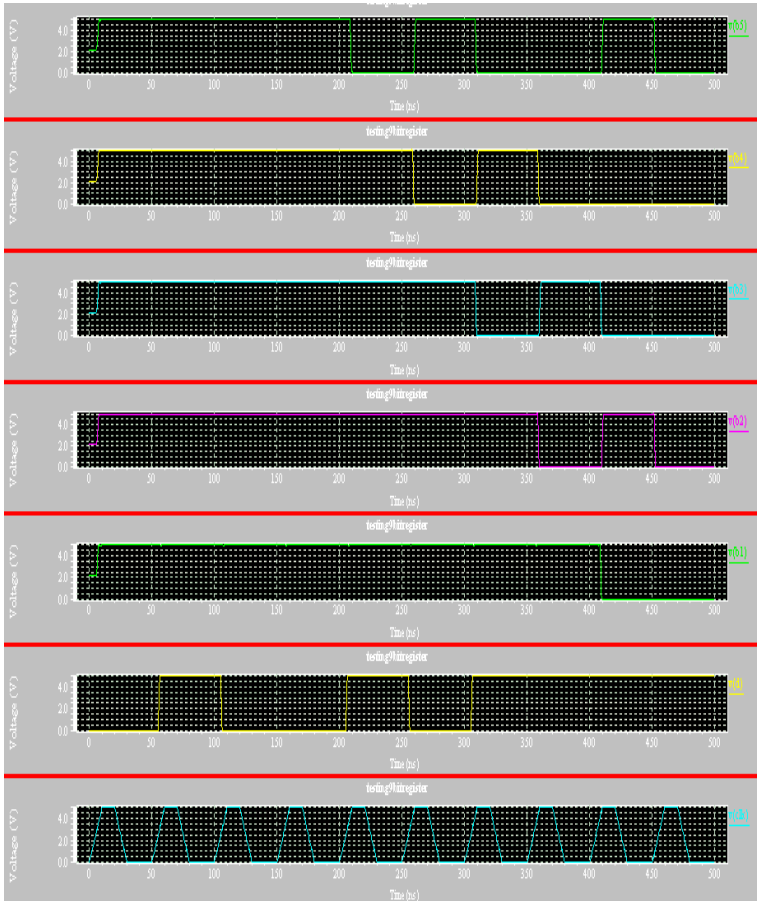
NODE NAME	NUMBER
GND	5
VDD	11
CLK	46
D	24
CLR	35
B1	192
B2	64
B3	70
B4	84
B5	101

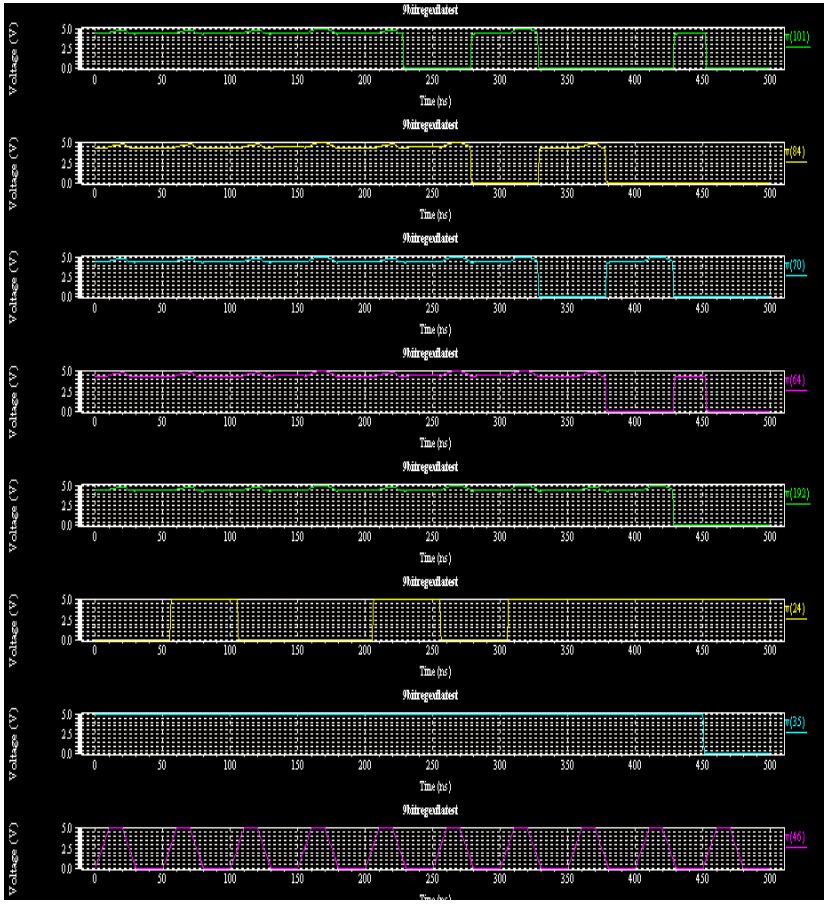
Layout Simulation of Header Register

- The Layout of the Header Register was extracted for simulation in TSpice.
- Node Numbers extracted were identified with the input and output nodes used in the simulation
- A Comparison of the S.Edit simulation vis.a.vis the .8uHP tech simulation is shown.



S.Edit Vs. L.Edit Simulation





Summary

- Functional Modules were identified and simulated.
- The Counter required by the Controller was implemented and simulated.
- The decision logic of the Controller was identified.
- A State diagram based approach for the individual modules is more rigorous and complete and has not been extensively explored.
- Layout simulation of the 9 bit Register was made using the 0.8uHP technology