Router Chip

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Abstract

The router chip project involves the design of modules that interleaves both combination and sequential circuits. The chip has a serial interface for the incoming data. The chip has 4 destination ports to route the incoming packets RT0 through RT3 based on the address field in the packet header. The maximum packet size the router can handle is 17bits, it comprises of 8 data bits and 9 overhead header bits. The chip is to function with a clock of 100 MHz – 10ns period. The chip provides a FIFO based buffering of up to 4 incoming packets whose destination ports are busy. If the buffers overflow the chip asserts its SS Busy signal to deny service till queue is emptied. For detailed specifications see Annex-A.

The main modules that make up the chip are the control module, FIFO buffers, counters, Multiplexers and Decoders. The overall logic for the routing function was identified and the individual modules were built and simulated in Spice.

1. 0 Introduction

In this project we attempt at solving a problem that has been identified by the specifications which lists the requirements of the system.

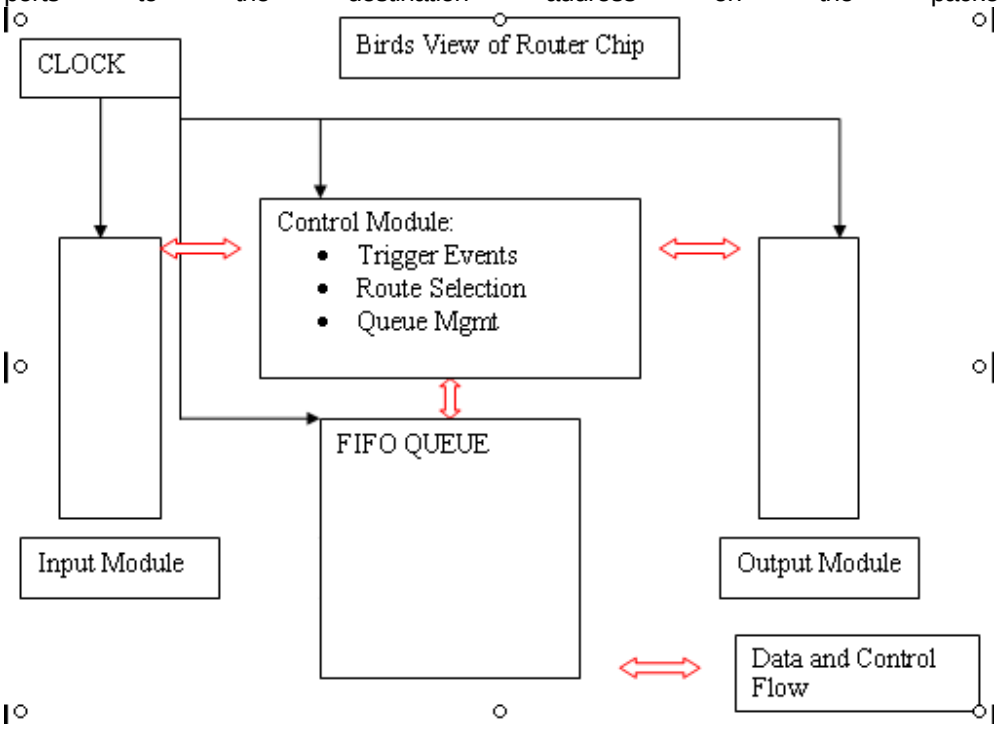
The crux of the project lies at identifying and personifying the required functionality into realizable circuit elements. The beauty of the process of engineering a product involves the organization of the subset of building blocks identified in the earlier ALU project, into modules that have a character, function and identity of purpose.

The Quality experts believe every process is a continuously evolving towards improvement, Japanese call it *Kaisen. Kaisen* aptly describes the design initiative. Hope the initiated cycle of design improves and refines with effort and initiative.

2. 0 Design

2.1 Router A Birds view

The Router has to have the following modules to direct the incoming packets to the respective destination. The header contains the address field that enables the router to lookup the destination port to switch the incoming stream. The router relies on the routing information, which are essentially look up tables. The tables map the available destination ports to the destination address on the packet.

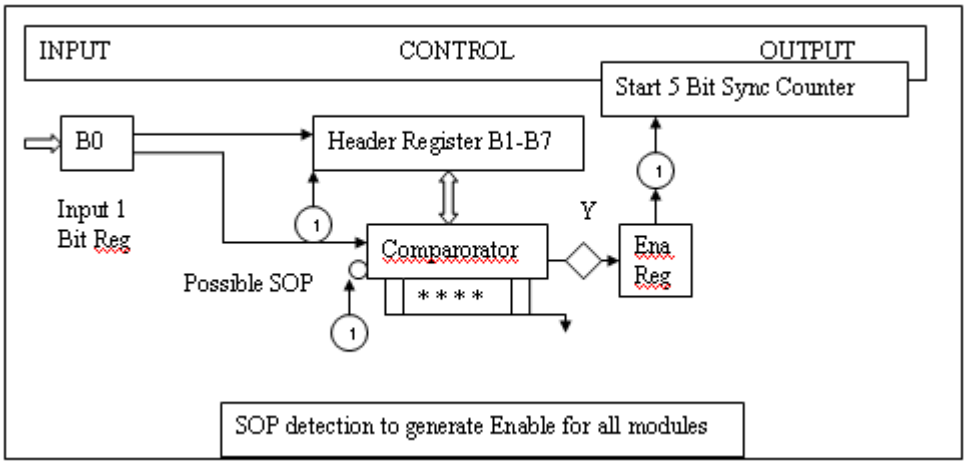


• Figure 1 Block Diagram - Router

- The Clock Module is responsible for the synchronization of Modular interaction and provide the reference timing for a sequence of events to be triggered in tandem.
- The Input and Output modules forms the interface to the external world the Router has a Serial interface i.e. bits stream in serially one after the other
- The Controller Module is the heart or brain of the system. It is responsible for the co-ordination and normal functioning of the router.
  - ✓ The Controller Triggers and Handles Events
  - ✓ Does the Lookup for Routing and Queuing
  - ✓ Generates signals (Enable) or controls data flow to accomplish the above tasks.

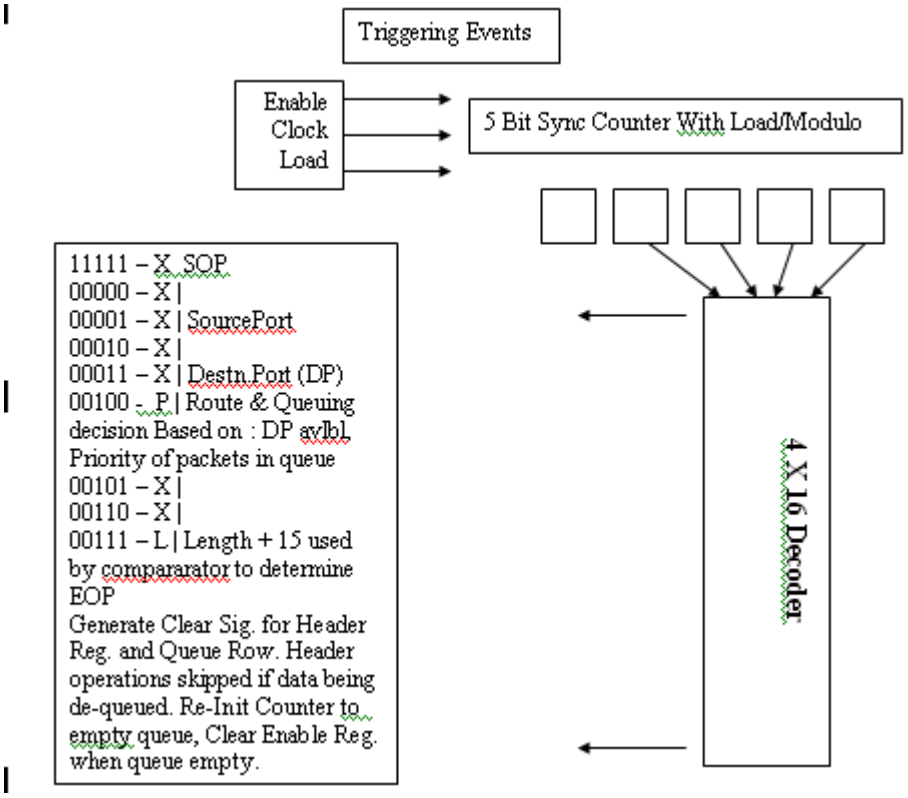
2.2 Detailed Design

2.2.1 Start Of Packet Triggered Events



- Figure 2 Start of Packet, Events triggered

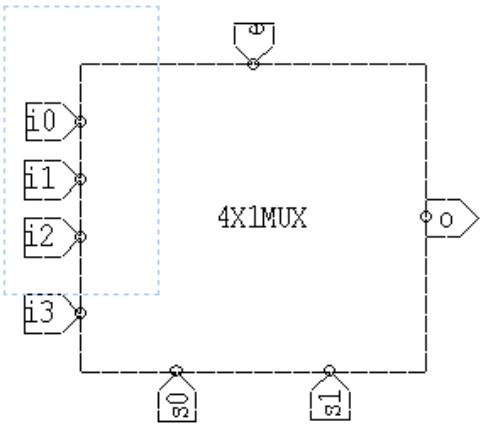
2.2.2 Clocked Events



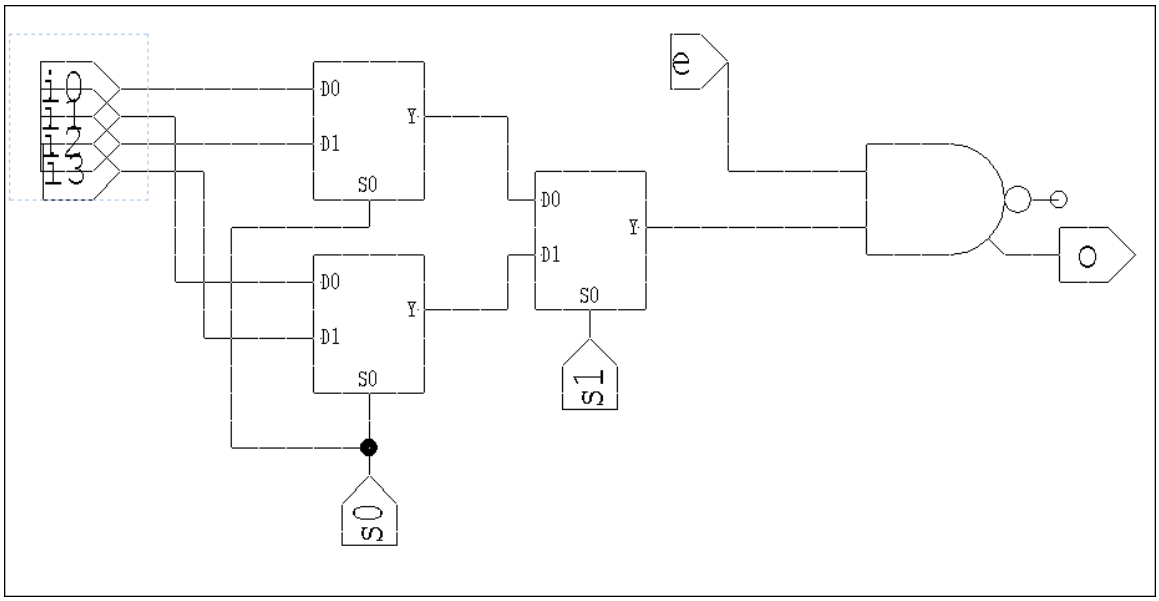
- Figure 3 Clock based Event Management

3.0 Modules, Test Cases and Simulation results

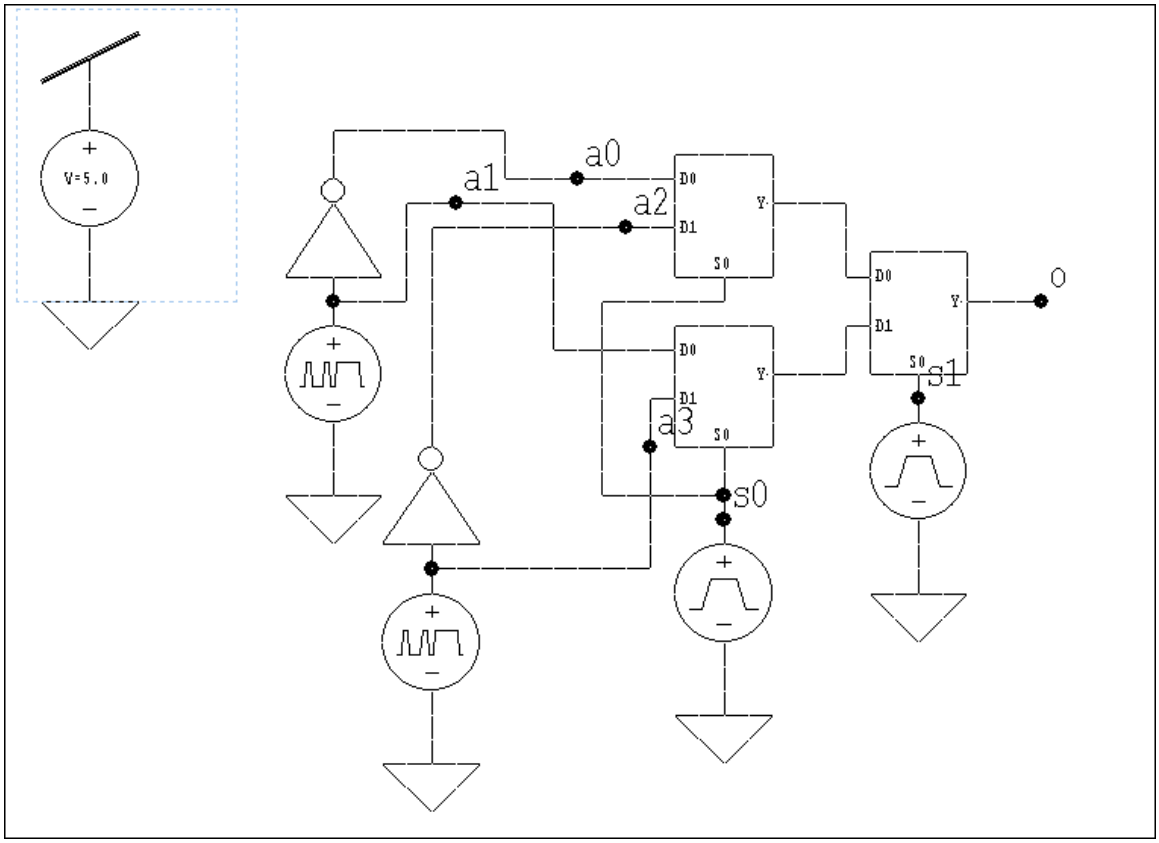
3.1 Multiplexer



- Figure 4 Multiplexer to control data flow between input/output stream and FIFO Queue

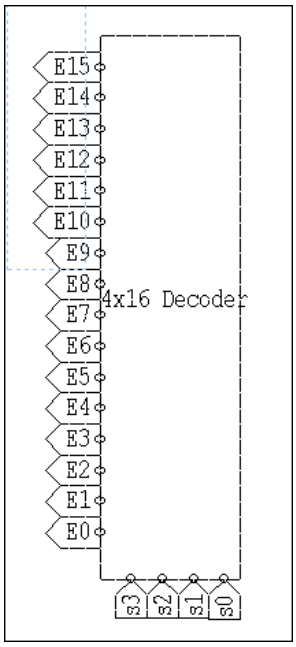


• Figure 5 Multiplexer Schematic

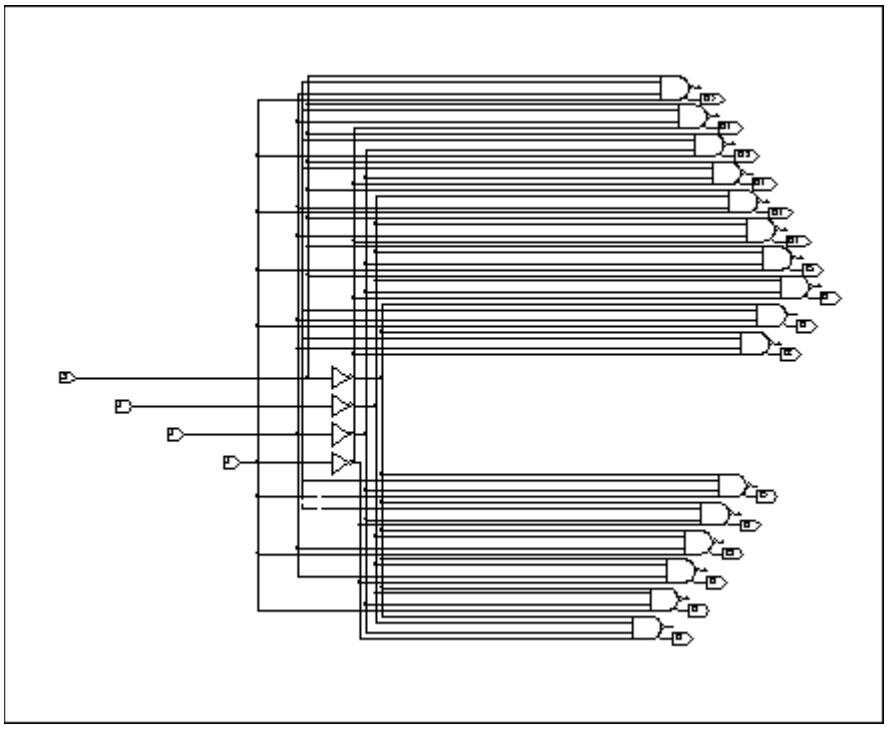


• Figure 6 Testing the Multiplexer

3.2 Decoder to generate Chip Enable

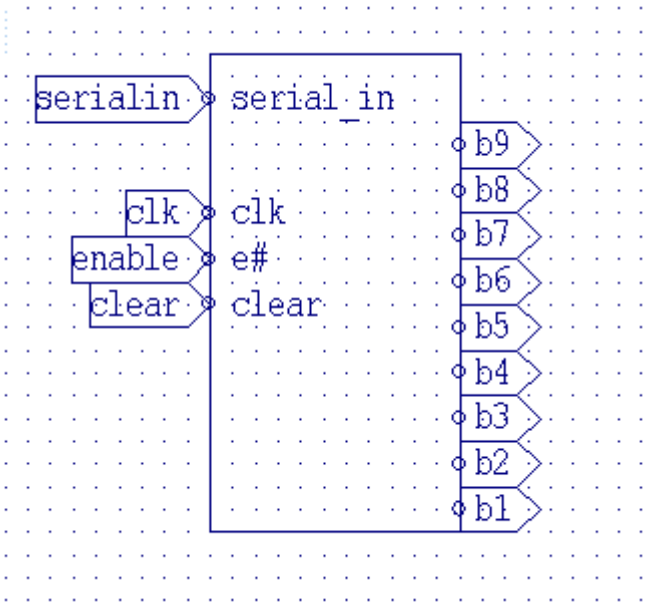


- Figure 7 Modified Decoder that generates Module-Enable signal.

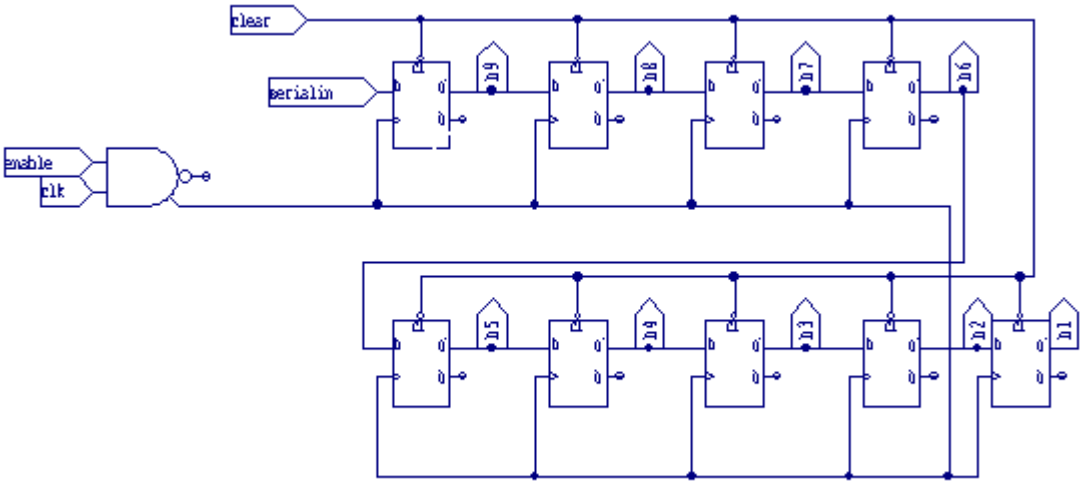


- Figure 8 Module Enable Decoder Schematic

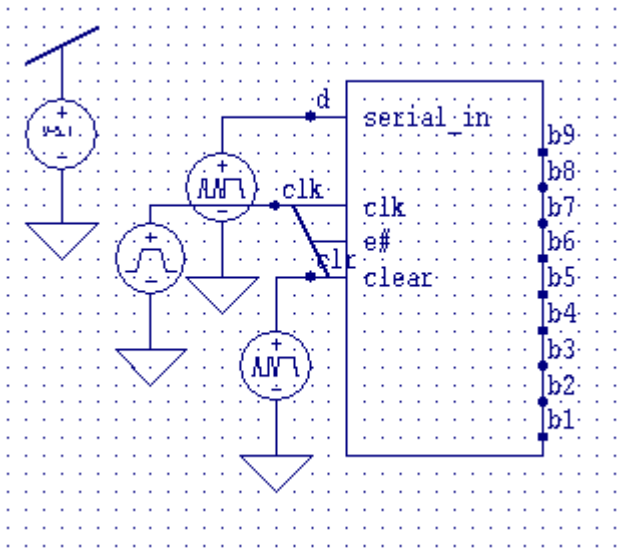
3.3 Nine Bit Header Register with Clear



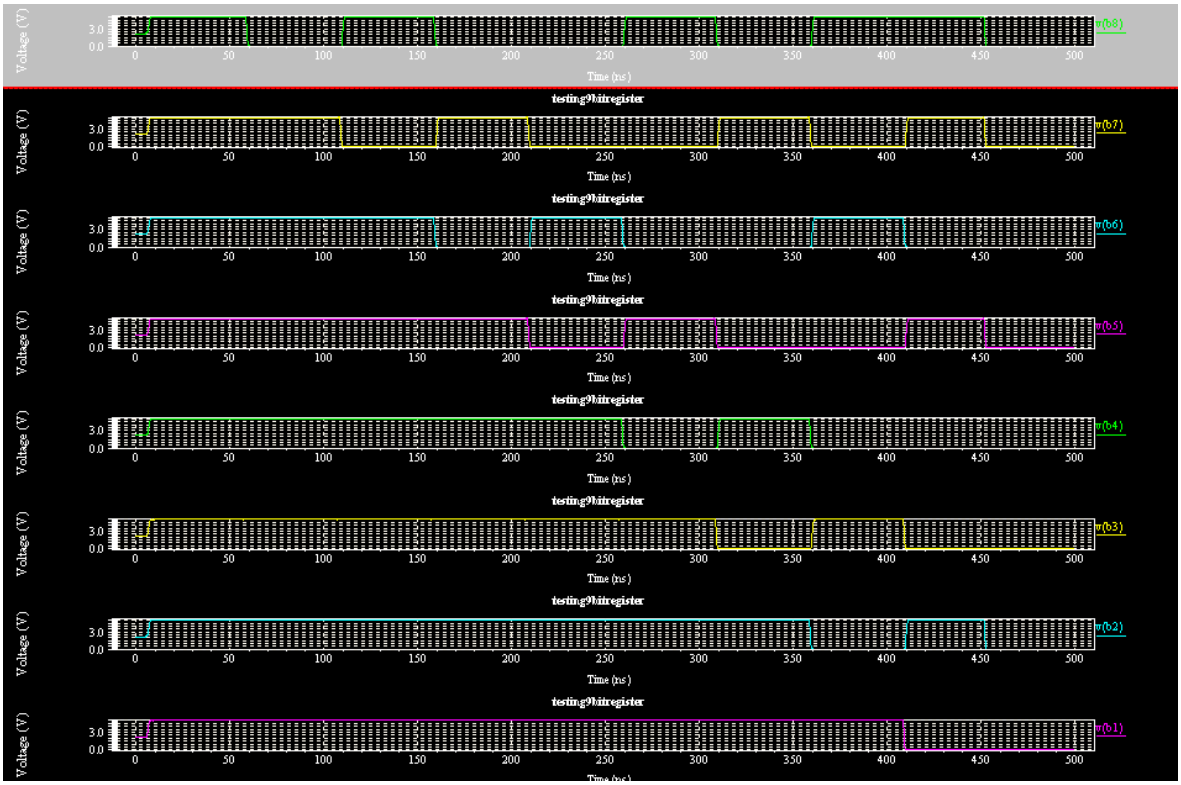
- Figure 9 Header Register Symbol



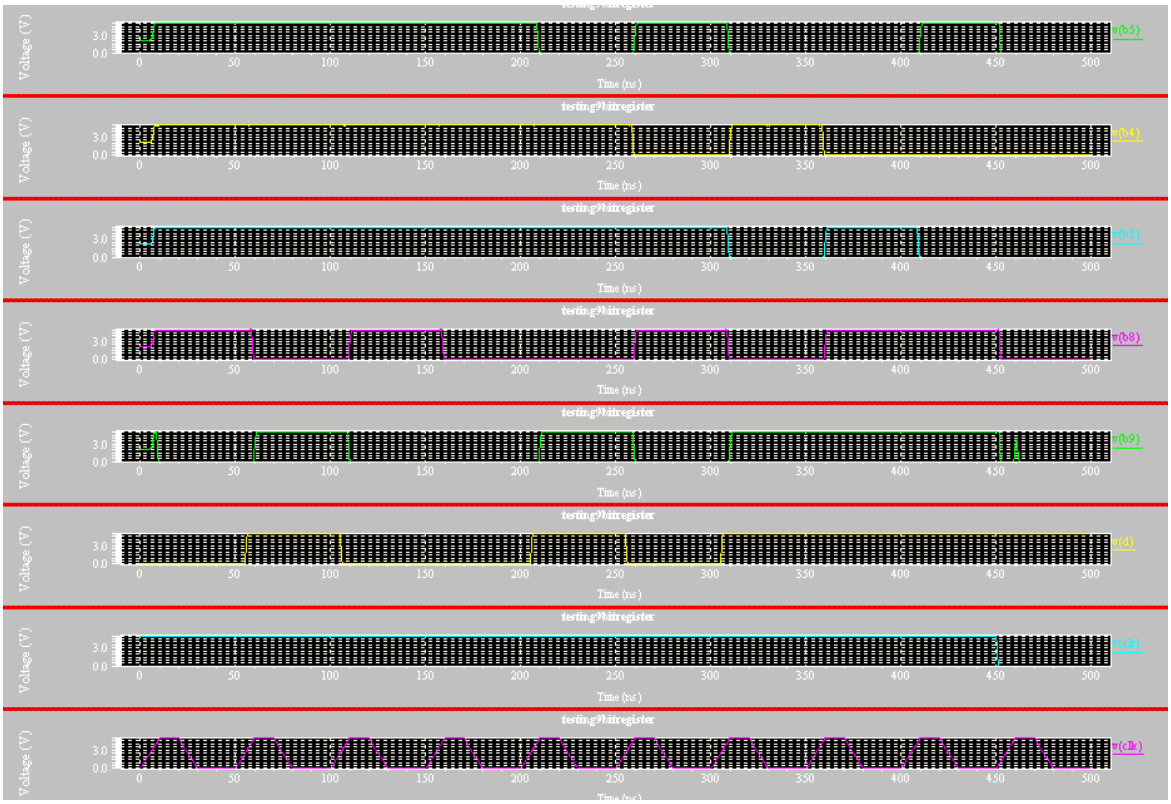
- Figure 10 Header Register with Clear and Parallel out



- Figure 11 Testing of Nine Bit Register

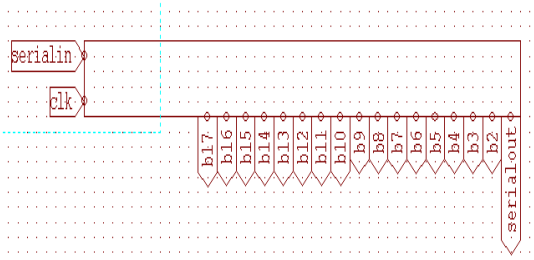


- Figure 12 Register with 9 bits of data after 9 Clocks

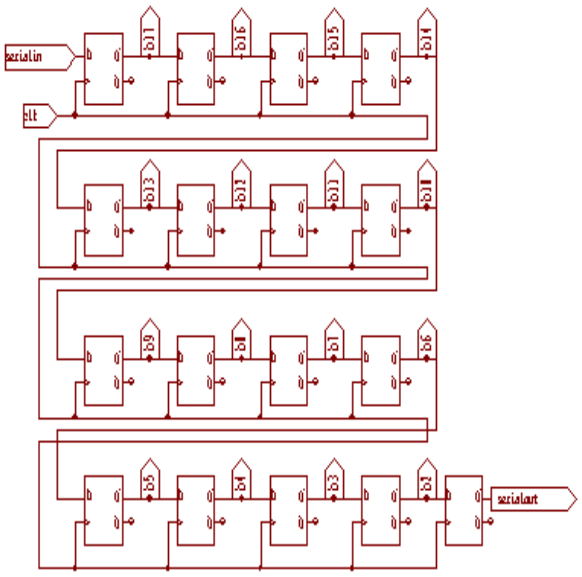


- Figure 13 Clearing Register Operation

3.4 17 Bit Queue Bank

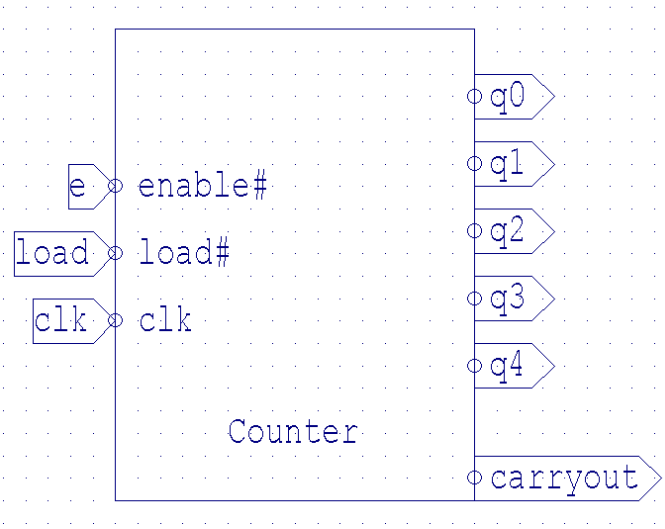


- Figure 14 Symbol of 17 bit Register Bank

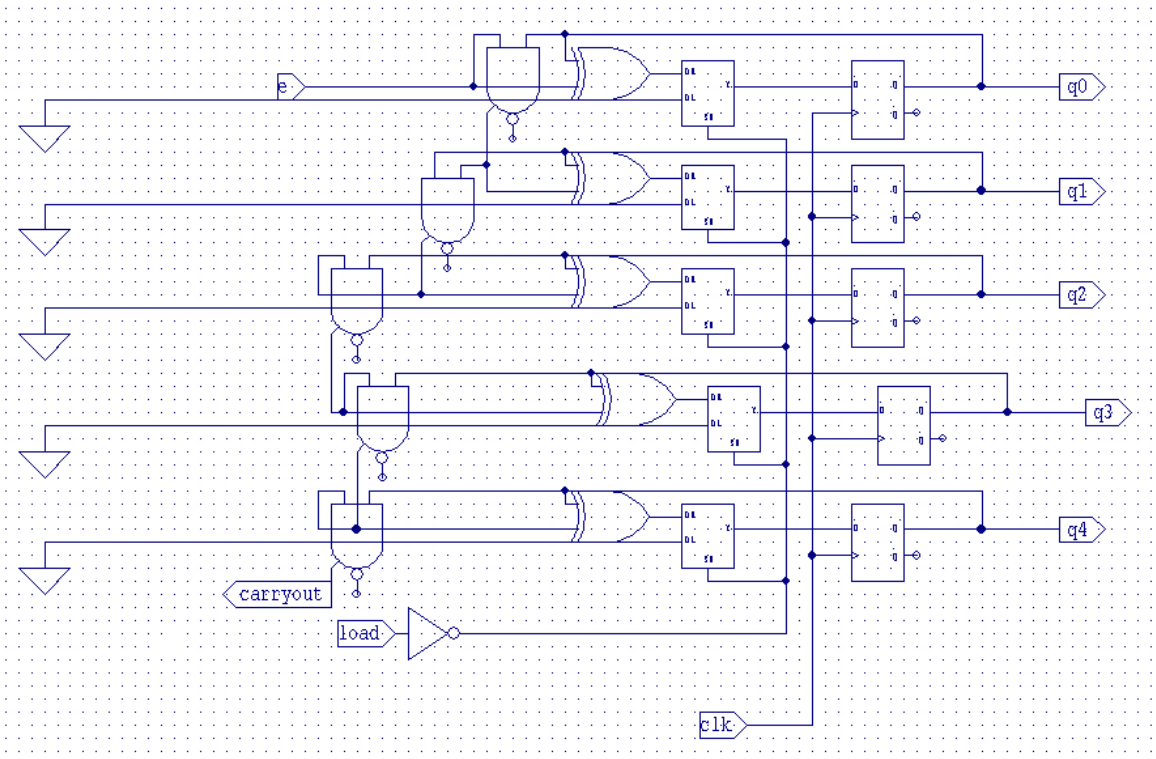


• Figure 155 Register Bank Schematic

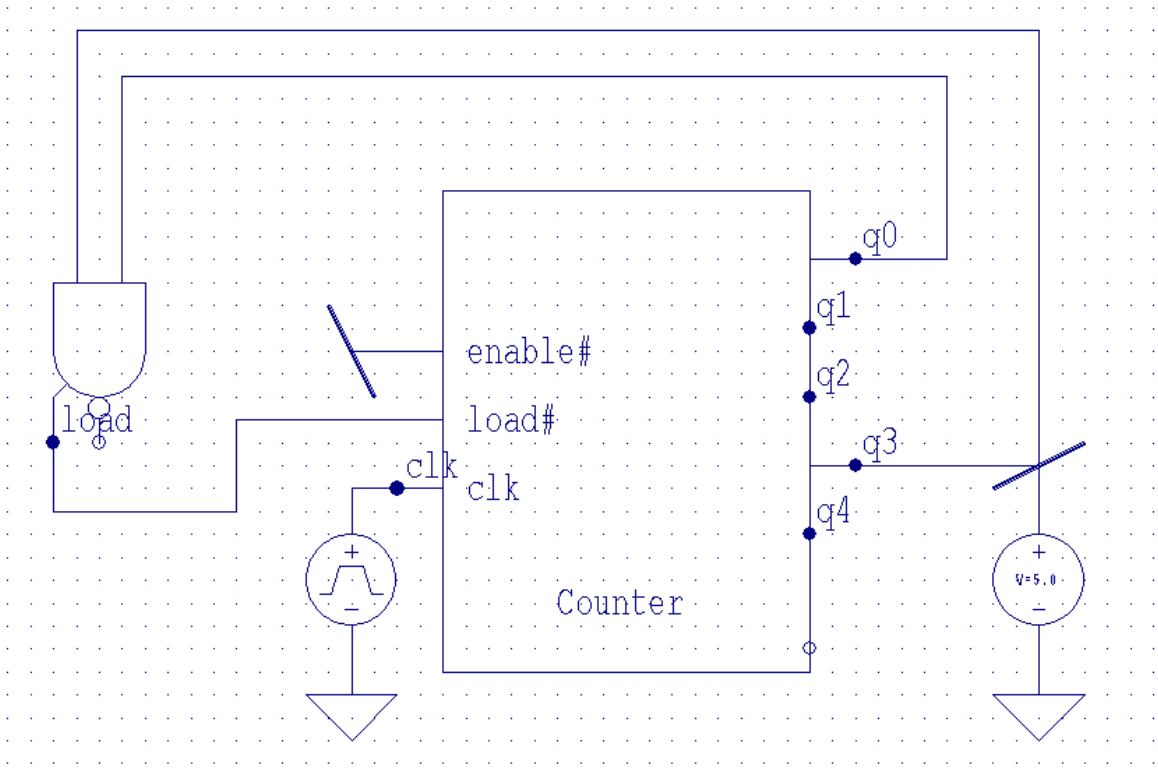
3.5 Five Bit Synchronous Counter with Modulo Operation



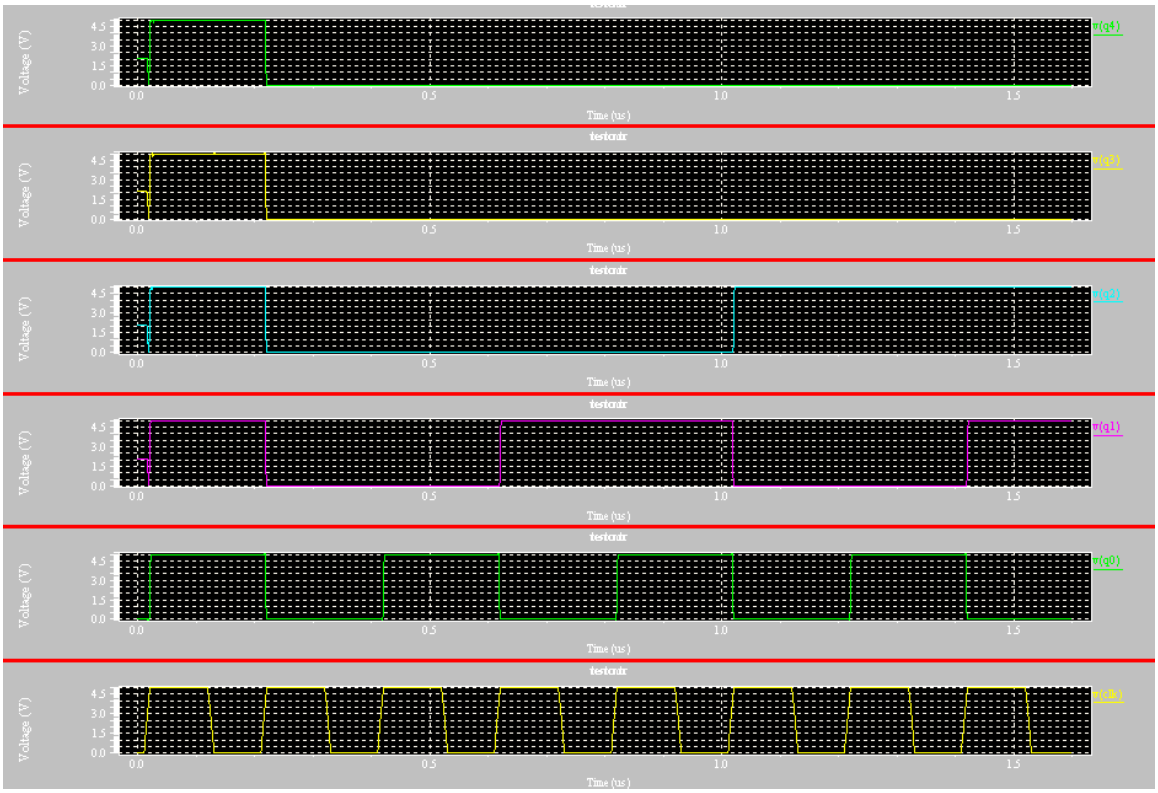
• Figure 16 Five Bit Synchronous Counter



• Figure 17 Five Bit Synchronous Counter - Schematic



• Figure 18 Modulo 10 counter



- Figure 19 Counter Waveform

4.0 Layout Simulation

4.1 Simulation of the 9 Bit Register Layout in Tspice

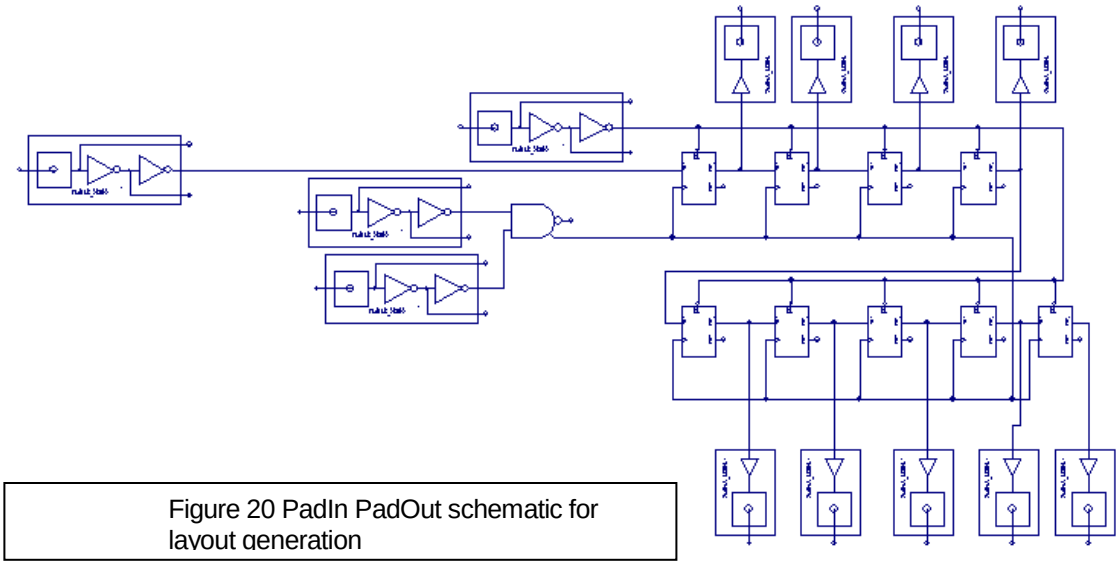


Figure 20 PadIn PadOut schematic for layout generation

4.2 Layout of 9 Bit Register

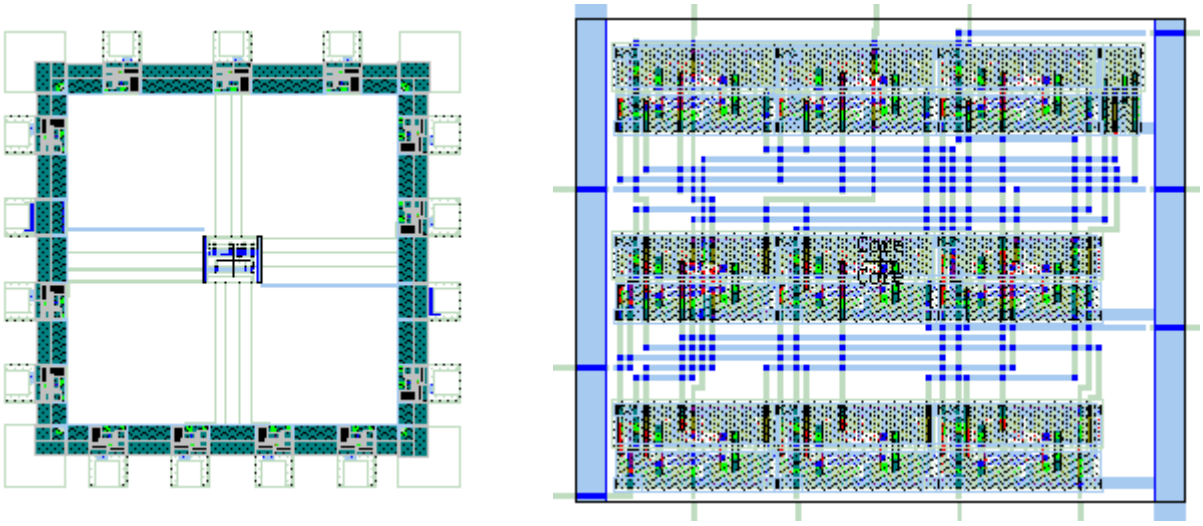
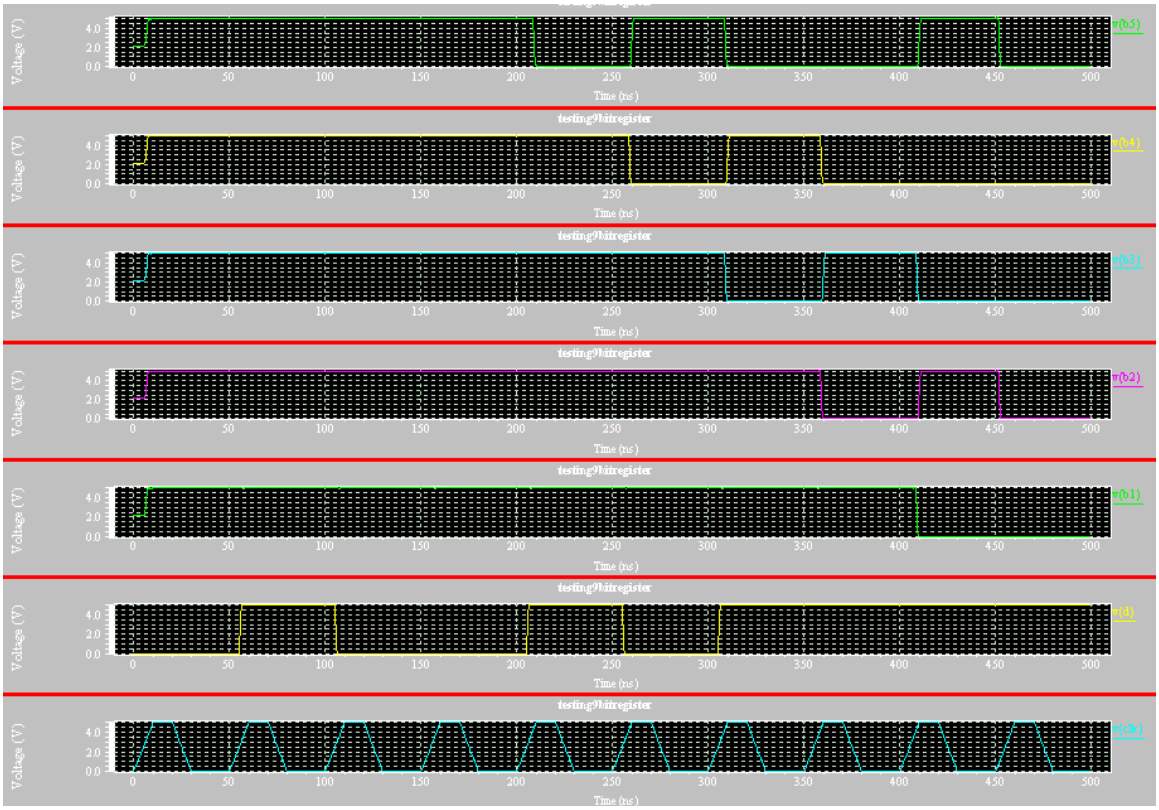
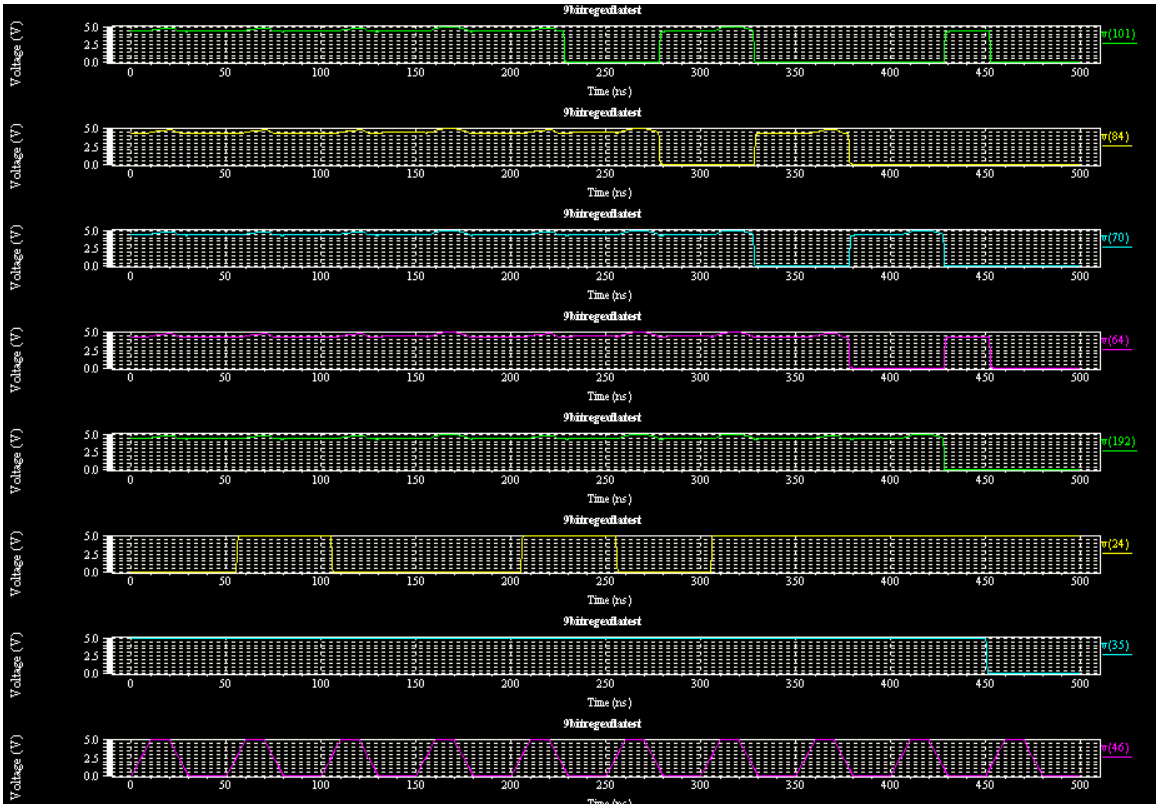


Figure 21 Padded and Core layout of Header Register

4.3 S.Edit Simulation Waveform Vs. LEdit Simulation





5.0 Scope and Conclusions

- ✓ Functional Modules were identified and simulated.
- ✓ The Counter required by the Controller was implemented and simulated.
- ✓ The decision logic of the Controller was identified. The decisions are based on the triggering event and the current state. The controller responds with an appropriate action in response to the stimuli. A State diagram based approach for the individual modules is more rigorous and complete and has not been extensively explored.
- ✓ Layout simulation of the 9 bit Register was made using the 0.8uHP technology file to compare the simulation results with what would be closer to the real world.

6.0 Annex

6.1 Specifications Document – A